REMARKS

Claims 1-20 are pending.

Claims 1-20 stand rejected.

Claims 1, 2, 4, 6, 7, 9, 11, 12, 17, and 20 have been amended.

I. Claim Rejections - 35 U.S.C. § 102

Claims 1-5, 7, 9, 10, and 20 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Applicant's admitted prior art (hereinafter "*APA*"). Applicant respectfully traverses the rejection.

Referring to Figure 1 of the *APA*, a decimation filter 106 performs a 2:1 sampling frequency reduction, i.e. from $2f_S$ to f_S. The delta sigma modulator 108 operates at frequency f_S, and, thus, the delta sigma modulator operating cycle is $1/f_S$. The loop filter 110 of delta sigma modulator 108 sequentially processes each input sample of an input signal received from the decimation filter 106. Furthermore, the loop filter 110 processes one input signal sample per delta sigma modulator cycle. Even assuming that the decimation filter 106 is part of the delta sigma modulator 108 and operates at the delta sigma modulator operating frequency f_S, each sample of the input signal to the decimation filter 106 is processed sequentially.

In contrast to the teachings and suggestions of the APA, Claim 1 recites a delta-sigma modulator having an internal filter, and "the internal filter comprises a second integrator, coupled to the first integrator, to process first and second input samples and the first integrator output signal **during a single cycle of the delta sigma modulator**, wherein the first and second input samples represent two successive-in-time samples of an input signal to the delta sigma modulator, the first and second input samples are modified by different gains prior to processing by the second integrator, and the cycle of the delta sigma modulator equals $1/f_s$." (emphasis added). Thus, rather than processing each input sample sequentially, the second integrator of the internal filter of Claim 1 processes "first and second [successive-in-time] input samples [of an input signal to the delta sigma modulator] and the first integrator output signal **during a single cycle of the delta sigma modulator**." Claim 1. (emphasis added).

Also in contrast to the teachings and suggestions of the APA, Claim 7 recites "during one delta sigma modulator cycle equal to 1/*f*, updating a second integrator with (i) the first gain modified input data sample, (ii) the second gain modified input data sample, and (iii) the first integrator output signal" and "the first and second input data samples are successive-in-time data samples of the received input data." Claim 7. (emphasis added).

Similarly, in contrast to the teachings and suggestions of the APA, Claim 20 recites "means for updating a second integrator with (i) the first gain modified input data sample, (ii) the second gain modified input data sample, and (iii) the first integrator output signal during one delta sigma modulator cycle equal to 1/*f*" and "the first and second input data samples are successive-in-time data samples of the received input data." Claim 20. (emphasis added).

Accordingly, for at least the above reasons, Applicant respectfully requests withdrawal of the rejection of independent Claims 1, 7, and 20. Also, for at least the above reasons, Applicant respectfully requests withdrawal of Claims 2-5 (dependent from Claim 1) and Claims 9 and 10 (dependent from Claim 7).

II. Claim Rejections - 35 U.S.C. § 103

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *APA* in view of U.S. Patent No. 6,271,782 issued to Steensgard-Madsen (hereinafter "*Steensgard-Madsen*").

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *APA* in view of U.S. Patent No. 6,433,726 issued to Fan (hereinafter "*Fan*").

Fan discloses a quadrature ADC delta sigma modulator with a primary function of sample rate conversion. Referring to Figures 1 and 2 of *Fan*, the ADC delta sigma modulator 100 has an operating frequency (e.g. 91.8 MHz) that is different than the output sample rate (e.g. 9.8304 MHz). Figure 2 indicates the accumulator 230 of decimator 130 using the input sample clock frequency = F1 while the output sample rate frequency = F2 = F1/(N+P/Q).

Steensgard-Madsen includes a delta sigma modulator system in Figure 8 that includes three integrators following respective nodes 116, 118, and 120. The input signal g(k) is modified by two gains $\alpha1$ and $\alpha2$ before being provided to two of the integrators. Nevertheless, each integrator of *Steensgard-Madsen* processes only one input signal sample, as modified by two gains α1 and α2, per cycle of the delta sigma modulator. In contrast to teachings and suggestions of *Steensgard-Madsen* in view of *Fan*, Claim 1, from which Claim 6 depends, recites "a second integrator, coupled to the first integrator, to process first and second input samples and the first integrator output signal **during a single cycle of the delta sigma modulator**, wherein the first and second input samples represent two successive-in-time samples of an input signal to the delta sigma modulator, the first and second input samples are modified by different gains prior to processing by the second integrator, and the cycle of the delta sigma modulator equals $1/f_s$." Claim 1. (emphasis added).

Accordingly, Applicant respectfully requests withdrawal of the rejection of Claim 6.

III. Claim Rejections - 35 U.S.C. § 102

Claim 11 stands rejected under 35 U.S.C. § 102(a) as being anticipated by *APA*. Applicant respectfully traverses the rejection.

Referring to Figure 1 of the *APA*, a decimation filter 106 performs a 2:1 reduction in a sampling frequency of a signal, i.e. from $2f_S$ to f_S. The delta sigma modulator 108 operates at frequency f_S, and, thus, the delta sigma modulator operating cycle is $1/f_S$. Integrators of the loop filter 110 of delta sigma modulator 108 are sequentially updated with each input sample from the decimation filter 106. Furthermore, the loop filter 110 processes one input signal sample per delta sigma modulator cycle. Even assuming that the decimation filter 106 is part of the delta sigma modulator 108 and operates at the delta sigma modulator operating frequency f_S, each input signal to the decimation filter 106 is processed sequentially.

In contrast to the teachings and suggestions of the APA, Claim 11 recites a method of modulating input data sampled at M times a frequency f_s (Mf_s) using a delta-sigma modulator operating at frequency f_s, and "converting the input data into low pass filtered data comprises during one delta sigma modulator cycle equal to $1/f_s$, updating a second integrator with (i) the first gain modified input data sample, (ii) the second gain modified input data sample, and (iii) the first integrator output signal" and "the first and second input data samples are successive-in-time data samples of the received input data" (emphasis added). Thus, rather than updating an integrator with input samples sequentially, Claim 11 recites "during one delta sigma modulator cycle equal to $1/f_s$, updating a second integrator with (i) the first gain modified input data sample, (ii) the second gain modified input data sample, and (iii) the first integrator output signal." Claim 11. (emphasis added).

Accordingly, for at least the above reasons, Applicant respectfully requests withdrawal of the rejection of independent Claim 11.

IV. Claim Rejections - 35 U.S.C. § 103

Claims 12-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *APA* in view of *Steensgaard-Madsen*. Applicant respectfully traverses the rejection.

Claims 12-16 depend from Claim 11. Thus, for at least the same reasons set forth above regarding Claim 11, Applicants respectfully request withdrawal of the rejection of Claims 12-16.

IV. Claim Rejections - 35 U.S.C. § 103

Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Fan* in view of *Steensgaard-Madsen*. Applicant respectfully traverses the rejection.

As previously set forth, *Fan* discloses a quadrature ADC delta sigma modulator with a primary function of sample rate conversion. Referring to Figures 1 and 2 of *Fan*, the ADC delta sigma modulator 100 has an operating frequency (e.g. 91.8 MHz) that is different than the output sample rate (e.g. 9.8304 MHz). Figure 2 indicates the accumulator 230 of decimator 130 using the input sample clock frequency = F1 while the output sample rate frequency = F2 = F1/(N+P/Q).

Also as previously set forth, *Steensgard-Madsen* includes a delta sigma modulator system in Figure 8 that includes three integrators following respective nodes 116, 118, and 120. The input signal g(k) is modified by two gains $\alpha1$ and $\alpha2$ before being provided to two of the integrators. Nevertheless, each integrator of *Steensgard-Madsen* processes only one input signal sample, as modified by two gains $\alpha1$ and $\alpha2$, per cycle of the delta sigma modulator.

In contrast to teachings and suggestions of *Steensgard-Madsen* in view of *Fan*, Claim 17 recites “during one delta sigma modulator cycle, providing the first and second data samples modified by the respective second and fourth gains, second quantizer feedback, and output data from the first integrator to a second integrator”, “wherein the first and second data samples are successive-in-time samples of the input signal~~,~~” Claim 17. (emphasis added).

Accordingly, Applicant respectfully requests withdrawal of the rejection of Claim 17.

V. Claim Rejections - 35 U.S.C. § 103

Claims 18 and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Fan* in view of *Steensgaard-Madsen* as applied to claim 17, and further in view of *APA*. Applicant respectfully traverses the rejection.

Claims 18-19 depend from Claim 17. Thus, for at least the same reasons set forth above regarding Claim 17, Applicants respectfully request withdrawal of the rejection of Claims 18-19.

CONCLUSION

In view of the amendments and remarks set forth herein, Applicant respectfully submits that all pending claims are in condition for allowance. Accordingly, Applicant requests that a Notice of Allowance be issued. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is requested to telephone the undersigned at 512-338-9100.

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Respectfully submitted,

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